

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-13. (Cancelled)

14. (Previously Presented) A method for accessing internal memory of a disk controller, comprising:

storing disk controller control data on a first memory that is located on the disk controller;

requesting the control data from the first memory; and

transferring the control data from the first memory to a second memory, wherein the second memory is located on a test access port controller and the test access port controller is located on the disk controller.

15. (Previously Presented) The method of claim 14 further comprising transferring the control data from the second memory to a device that is external to the disk controller.

16. (Previously Presented) The method of claim 14 further comprising loading at least one of a write instruction, a read instruction, and a memory address that corresponds to the first memory into the second memory.

17. (Previously Presented) The method of claim 14 further comprising providing access to the first memory with an arbitration module.

18. (Previously Presented) The method of claim 14 wherein at least one of the first memory and the second memory is a register.

19. (Previously Presented) The method of claim 14 further comprising:
writing data to the first memory; and
subsequently writing the data to the second memory.

20. (Previously Presented) The method of claim 14 further comprising:
loading a read command in the second memory;
loading an address of the first memory in the second memory;
transferring the control data from the first memory to the second memory according to the read command and the address.

21. (Previously Presented) The method of claim 14, further comprising acquiring access to the second memory using an arbitration module.

22. (Previously Presented) A disk controller comprising:
a first memory that stores disk controller control data;
a test access port controller that communicates with the first memory; and
a second memory that is located on the test access port controller,

wherein the test access port controller receives a request for the control data from a device that is external to the disk controller and transfers the control data from the first memory to the second memory.

23. (Previously Presented) The disk controller of claim 22 wherein the test access port controller transfers the control data from the second memory to the device.

24. (Previously Presented) The disk controller of claim 22 wherein the test access port controller loads at least one of a write instruction, a read instruction, and a memory address that corresponds to the first memory into the second memory.

25. (Previously Presented) The disk controller of claim 22 further comprising an arbitration module that receives a request from the test access port controller to access the first memory.

26. (Previously Presented) The disk controller of claim 22 wherein at least one of the first memory and the second memory is a register.

27. (Previously Presented) The disk controller of claim 22 wherein the test access port controller writes data to the first memory and subsequently writes the data to the second memory.

28. (Previously Presented) The disk controller of claim 22 wherein the test access port controller loads a read command in the second memory, loads an address

of the first memory in the second memory, and transfers the control data from the first memory to the second memory according to the read command and the address.

29. (Previously Presented) A disk controller comprising:
first memory means for storing disk controller control data;
test access port controller means for communicating with the first memory;
and
second memory means that is located on the test access port controller means,
wherein the test access port controller means receives a request for the control data from a device that is external to the disk controller and transfers the control data from the first memory means to the second memory means.

30. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means transfers the control data from the second memory means to the device.

31. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means loads at least one of a write instruction, a read instruction, and a memory address that corresponds to the first memory means into the second memory means.

32. (Previously Presented) The disk controller of claim 29 further comprising arbitration means for receiving a request from the test access port controller means to access the first memory means.

33. (Previously Presented) The disk controller of claim 29 wherein at least one of the first memory means and the second memory means is a register.

34. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means writes data to the first memory means and subsequently writes the data to the second memory means.

35. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means loads a read command in the second memory means, loads an address of the first memory means in the second memory means, and transfers the control data from the first memory means to the second memory means according to the read command and the address.